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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,920	11/29/2002	Rolf-P. Vollertsen	2001P19578US	5321

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EXAMINER	
DEB, ANJAN K	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,920	VOLLERTSEN, ROLF-P.	
	Examiner	Art Unit	
	Anjan K Deb	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10, 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 4,904,946) in view of Bognar (US 5,150,059).

Re claims 1,10, 21-26 Hirai discloses method of reliability testing comprising a test structure 2 (Fig. 1-2) and determining a critical current of the test structure, wherein the critical breakdown current of the test structure causes a circuit to fail subjecting the test structure to stress conditions repetitively (varying electric stress)(column 2 lines 64-68, column 3 lines 1-7) as a function of time (t) (Fig. 1b, Fig. 2b), determining an operating current of the test structure, and recording a critical breakdown time (column 3 lines 39-44) when the operating current of the test structure is equal or smaller than the critical breakdown current.

Re claims 1,10, 21-26, Hirai did not expressly disclose measuring breakdown resistance.

Bognar (US 5,150,059) teaches measuring insulation resistance of test structure 6 by applying a test voltage and measuring current 26 (column 8 lines 1-5)(Fig.10).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Hirai by adding measuring resistance of test structure as a function of the measured voltage and current as disclosed by Bognar for determining the insulation resistance of test structure.

Re claims 2-6, Hirai discloses dielectric layer (thin film) formed on substrate (silicon wafer) (column 3 lines 17-21) comprising a capacitor structure 2 (Fig. 1).

Re claims 7-9, Hirai discloses stress testing comprising elevated voltage (voltage ramping) and elevated temperature (thermal history) or elevated current (current ramping)(column 3 lines 16-39).

Re claim 10, Hirai discloses determining critical breakdown current in a circuit environment under normal operating conditions (Fig. 5).

Re claim 10, Hirai did not expressly disclose determining the critical breakdown resistance in a circuit environment under normal operating conditions (Fig. 5) but would have been obvious to do so in view of Bognar (US 5,150,059).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Hirai by adding measuring resistance of test structure as a function of the measured voltage and current as disclosed by Bognar for determining the insulation resistance of test structure.

3. Claim 11-20, 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 4,904,946) and Bognar (US 5,150,059) in view of Amersekera et al. (US 5,949,694).

Re claims 11-20, 27-30, Hirai as modified by Bognar discloses all of the claimed limitations as set forth above for determining electrical property of test structure (sample insulating film) comprising voltage (electric stress)(V)(Fig. 1b) and electric current (Fig. 2b) after a time interval (t) and determining maximum current except expressly disclosing determining the critical breakdown resistance of test structure comprising a circuit simulation.

Amersekera et al. discloses determining the resistance R_{sub} of test structure (substrate) comprising a circuit simulation as a function of voltage V'_B and current I_{sub} (column 3 lines 21-30, column 6 lines 45-55, column 9 lines 43-67)(see also Figs. 2, 3 and 8 showing test structure).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Hirai and Bognar by adding determining the resistance of test structure comprising a circuit simulation as disclosed by Amersekera et al. for optimizing circuit on a substrate with regards to an overvoltage or ESD event (see abstract).

Pertinent Art

4 . The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kimura (US 5,594,349) discloses method of reliability testing comprising a test structure 11 (Fig. 1) having dielectric layer 11 formed on substrate 12 (Fig. 1) for dielectric breakdown prediction of test structure as a function of applied stress voltage and current (column 2 lines 13-

26)(Fig. 2) and for accurately predicting pressure resistance distribution of an insulating film (column 8 lines 23-28).

Kirihata et al. (US 6,326,800 B1) discloses test structure (Fig. 4) comprising insulating film (Tox) for reliability testing by repeatedly applying stress voltage (Vg) and detecting insulation breakdown (failure).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le, can be reached at (571) 272-2233.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone numbers are (703)-308-0956 and (703)-305-4900.

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2/19/04

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